REMARKS

Claims 1-24 remain active in the Application. Claim 9-10, 13, 15, 22, and 25 have been amended without prejudice. Claims 1-8 have been withdrawn from consideration.

The Title of the present application has been amended to make it more descriptive.

Claims 10, 13-15 and 21-24 stand objected to because of certain informalities.

In response, Applicants have now made the necessary corrections.

Claims 9-11, 13-15, 21 and 24 stand rejected under 35 U.S.C. 103(e) as being unpatentable over Jennion et al. (U.S.P No. 5,721,495) (Jennion) in view of Teene (U.S.P. No. 5,726,997).

Applicants respectfully traverse the above rejection for the following reasons:

1) Jennion teaches a circuit on a test board which makes a selection between power sources in order to power the voltage connection (Fig.1, 105) to the DUT. One power source can supply high current/ power as required for the switching operation of the DUT. The other power supply provides electronics for precisely measuring the current. Jennion does not teach nor suggest a separate quiescent power distribution, which is a key element of the Applicant's teaching.

2) Jennion teaches further a chip (DUT) being a single voltage island. In contradistinction, Applicant teaches that on-chip (on-DUT)voltage islands which can be selectively removed from the on-chip global power distribution. Jennion makes no provision to deselect a voltage island from the global power distribution. An IDDQ measurement for the on-chip circuitry outside of voltage islands is not possible with Jennion. Jennion further teaches a circuit and methodology for using that circuit to make a precise IDDQ current measurement at a power connection to a chip, which teaches away from Applicant.

3) The second cited reference Teene teaches moving a testing apparatus from the test equipment and test fixturing external to a chip (DUT) directly onto the chip. The Office Action erroneously identifies the Vss supply (16) and Vss internal (14) segments of the power rail in the chip as separate voltage busses. Teene teaches 16 and 14 as part of the power grid distribution of the power grid of the integrated circuit. In Teene's Figs. 2-4, the circuit implementations show 16 connected to 14 through a series connection in the monitoring cell. For example, Fig. 2 shows that current flowing from Vss supply 16 through bypass transistor 44 to Vss internal 14 or from 16 via 32 through current sensor transistor 26 via 38 to 14. In Fig. 3, a current divider implementation is used to reduce the impact of the current sensor on the power grid performance. In Fig. 4, a single instance of the current sensor and comparator is placed on-chip (instead of multiple copies in each current monitoring cell), and selection circuitry is added to the design to route local currents to the current sensor. Teene, by definition is implemented for a single power distribution. Teene makes no provision for voltages islands, which are islands of chip circuits that can be connected or disconnected from the power grid. Fig. 1 demonstrates these two points. In Fig. 1, chip circuits (standard cell or gate array) are shown being powered through a single power grid and multiple current monitoring cells. If a particular monitoring cell was open, then current would flow to the adjacent chip circuits through another monitoring cell. In contrast, Applicants teach performing a test by taking actual IDDQ current measurements, enables more complex IDDQ testing scenarios. Teene does not.

4) The Office Action states that by combining Jennion and Teene, allegedly renders Claim 9 unpatentable. Applicants traverse this assertion for the following reasons:

a) Teene does not teach separate global and quiescent power supply busses within the chip. Teene's Figs. 2-4 show that the Vss supply (16) and the Vss internal supply (14) are electrically connected and are part of the same power buss. The

combination of Jennion and Teene does not teach separate global and quiescent power supply busses within the chip.

b) Combining Jennion and Teene is not operable. Further, the two aforementioned teaching are redundant and do not complement each other. Jennion performs IDDQ testing of an IC using external test circuitry. Teene moves the current sensing operation and circuitry on to the IC, performing on-chip IDDQ testing.

c) The combination of Jennion with Teene does not teach a quiescent voltage buss and power distribution within the chip. Jennion selects a power supply-to-source power for a single voltage power connection to the chip. Teene does not apply, because it pertains to single power grid.

Rejection of Claim 10.

Neither Jennion nor Teene whether individually or in combination teaches this claim, as explained for the rejection of claim 9 *supra*. Furthermore, Applicant's teaching of hot switching is purposely required to effectively make IDDQ measurements for different voltage island combinations without having to reapply the conditioning test pattern. The combination of Jennion to Teene is unable to achieve this.

Rejection of Claim 11.

Neither Jennion nor Teene whether individually or in combination teaches this claim, as teached for the rejection of claim 9 *supra*. Applicants teach two separate voltage connections (power planes) and voltage distribution networks within the chip, which may be connected to two independent voltages supplied by two different power supplies. The combination of Jennion and Teene does not.

Rejection of Claims 13 – 14.

Neither Jennion nor Teene whether individually or in combination teaches this claim, as teached for the rejection of claim 9 *supra*.. Applicant teaches a header device, and not an

input connection to a select circuit, as the Office Action indicates. A header device as shown in Applicant's Fig. 1 (H1, H2, … , Hn) is a device that connects voltage islands (sinks) to the power distribution. Either the voltage island is powered through the header device or is not. Connections 116, 118, 120, 122 in Jennion are not header devices. Jennion test circuit 126 is used to select between power sources (inputs 116, 118, 120, 122) not sinks. The sink in Jennion is power plane 105.

Appplicant respectfully submits that the rejection of claims 10 through 15 is believed to be unwarranted, since Claims 10 through 15 depend on Claim 9 which Applicant believes to be patentable under 35 U.S.C. 103(a) over the combination of Jennion and Teene. Since the aforementioned combination does not render Claim 9 unpatentable, neither does the combination render all the dependent claims of claim 9 unpatentable.

Thus, Applicant believes that the rejection of claim 9-15 is patentable under 35 U.S.C. 103(a) over Jennion in view of Teene, and respectfully request that the Examiner reconsider and withdraw the stated rejection.

Claims 12 and 22 stand rejected under 35 U.S.C. 103(a) over Jennion in view of Teene and further in view of Akiki (U.S.P. No. 5,294,883) (Akiki).

Applicant submits that Akiki teaches away from Applicant's teaching. Akiki teaches a circuit that is limited to BiCMOS chips (circuits contain both CMOS and bipolar transistors). In BiCMOS circuits, there is DC current when the circuits are not switching. This DC current adds to the chip quiescent leakage current, which increases the IDDQ. The basis of IDDQ testing is to detect elevated leakage current due to defects. If the DC current paths are not disabled during IDDQ test, the DC current may compromise the sensitivity of the IDDQ test and not be able to resolve defect caused current against the high current component associated with bipolar good operation. Akiki's circuit detects when the IDDQ test is being enabled and shuts off the DC current associated with normal bipolar operation. BiCMOS circuits require two power rails (VDD and VTT). The predetermined test condition for IDDQ test is reducing the

voltage difference between VDD and VTT to within a predefined number. The disclosed circuit then shuts off the DC currents and IDDQ testing may be performed.

Applicant teaches that when voltage islands are hot-switched between VDDg and VDDq at different voltages, there will be a settling time needed to reach quiescence. If VDDg and VDDq are at the same voltage, the transition time will be minimized. Claims 12 and 22 are made to capture this feature. Akiki uses setting the two "global" rails to the same voltage as a signal to the shutoff circuits to disable DC leakage. Akiki's VTT is not a quiescent power bus. IDDQ testing under Akiki is performed to determine the IDDQ sourced from the VDD power supply. Thus, Akiki is believed to be unrelated to Applicant's teaching.

Accordingly, Applicant submits that Akiki in combination with Jennion and Teene does not render claims12 and 22 unpatentable since Akiki's teaching does not apply to Applicant's teaching as recited in claims 12 and 22, and further when combined with Jennion in combination with Teene, the combination of the tree references being inoperable as demonstrated *supra*.

Thus, Applicant believes that the rejection of claim 12 and 22 is patentable under 35 U.S.C. 103(a) over Jennion in view of Teene and further in view of Akiki, and respectfully request that the Examiner reconsider and withdraw the stated rejection.

Rejection of Claims 16 and 18.
Regarding the rejection of Claim 16, Applicant submits that Claim 16 depends on the now amended Claim 9, which, as shown *supra*, is deemed patentable over Jennion in combination with Teene.

Furthermore, Sugasawara teaches measuring IDDQ for regions with a chip within the context of the invention; however, the structure and methodology are different from those taught by Applicant. As Sugasawara points out, failure analysis (FA) defect isolation techniques include cutting the chip into sections and trying to test sections to

isolate the section that contains the defect. Sugasawara teaches an integrated chip configuration that supports coupling and decoupling circuit sections from a unitary power supply line (VDD) and providing power via selectable power supply lines (Fig. 1 VDD1, VDD2 and Fig. 2 SVDD). Figures1 and 2 show that a shared power supply scheme is embodied as well as reflected in the claims. This emulates the cutting and probing in an FA laboratory. Sections being tested are not "hot switched" between power supply lines, but routed to or from shared power supply connections (e.g., Figure 2 section 52 is supplied power from both 34 and 36 power supply lines, or decoupled from 34 and powered from 36).

Applicant teaches hot switching to source power from one of two different power busses (VDDg or VDDq) for IDDQ testing. Voltage islands are connected via separate header devices for each voltage island and voltage bus. Extending Jennion-Teene with Sugasawara for multiple sections requires additional power supplies and selectable power supply lines, which is quite different from Applicant (see Sugasawara col. 5 lines 22 – 26). Applicant can support many voltage islands with only two voltage busses.

Regarding the rejection of Claim 18, Sugasawara's teaching is described in the context of isolating defects in ICs to support failure analysis engineering, which the invention does providing the capability to IDDQ test a section or part of a region in the chip to further refine isolation. In contrast, Applicant teaches IDDQ testing on individual voltage islands or groups of voltage islands for additional purposes besides locating defects within the chip. For example, IDDQ testing at the individual voltage island level may be more desirable for a subset of the voltage islands on the chip due to their circuitry being more susceptible to certain defect types. It is not always necessary to isolate high IDDQ to the voltage island. Further, IDDQ measurements on groups may provide a faster way to IDDQ test, while still being sensitive to defective IDDQ levels, than testing each individual voltage island separately. These applications do not follow from Sugasawara. Testing individual or groups of voltage islands in Applicant is not obvious from Sugasawara in combination with Jennion and Teene

Rejection of Claim 17.

Regarding the rejection of Claim 16, Applicant submits that Claim 16 depends on the now amended Claim 9, which, as shown *supra*, is deemed patentable over Jennion in combination with Teene.

Applicant believes that Cole is being interpreted incorrectly by the Office Action. The Office Action cites Cole's col.7, lines 44-55. This citation is describing use of a resistive load placed between a chip output pin and ground to mimic a defect while using a defect-free IC in example 2. Cole does this to characterize the effect of current loading on the power source that is being used when the invention is being tested.

Rejection of Claims 19 and 20.

Regarding Claim 19, for the rejection in view of Sugasawara, please see Claims 16 and 18 above.

Inoshita is addressing the problem of detecting the presence of IDDQ due to a defect against the background IDDQ associated with normal chip leakage. Many newer technologies have high normal IDDQ and also have higher measurement variation. Inoshita discloses several ways to manipulate IDDQ measurements to make IDDQ tests more sensitive to the presence of defect related current and determine if a chip is defective. Applicant addresses this problem by improving the defect current to background current signal to noise ratio by reducing the amount of circuitry producing background current that is included in measurement. In addition, Applicant discloses using information about the voltage island contents to craft an IDDQ test metric consistent with the chip design. Claim 19 is taught in paragraph 0032 sections b, n, o, and p. For example, section b teaches comparing IDDQ measurements between different voltage islands with the same circuit content.

Rejection of Claim 20.

Regarding Sugasawara, please see Claims 16 and 18 above.

Applicant cannot find any reference in Inoshita to IDDQ measurements for similar circuitry, and thus, Applicant cannot place Inoshita teaching in its context, since Inoshita shows the invention chip connections and IDDQ test apparatus in Fig. 2 and a single power supply, making no provision for subdie current measurements. Inoshita teaches performing a chip level IDDQ average calculation for repeated IDDQ measurements. Applicant teaches performing an average measurement for subdie structures. In one embodiment, averaging IDDQ measurements from different voltage island instances with the same circuitry content.

Rejection of Claim 23.

Inoshita teaches IDDQ testing methods that have to do with taking several IDDQ measurements and processing the results to determine whether the IC being tested is defective. One example is the method of claim 2 which includes taking several IDDQ measurements on the same power bus, determining the maximum and minimum values measured, then determining if the IC is defective by comparing the difference between the maximum and minimum values to a predetermined value. This is often called a "delta" IDDQ test.

The Office Action cites Inoshita, Page 2, paragraphs 0011 and 0012 to show that Inoshita discloses locating IDDQ defects. In these paragraphs, which is part of the "Background of the Invention" section. IDDQ is defined as "the current value of the power source current (hereinafter called "a static-time power source current") that flows when the IC is out of operation". [0003] Paragraph 0011 teaches taking a series of IDDQ measurements and explains Fig. 14, which illustrates a timing chart of power source current versus time and indicates when IDDQ measurements would be taken using a conventional testing method. Paragraph 0012 teaches that the IDDQ measurements would be compared to a standard value of IDD. If one of the measurements was greater than the standard value the IC was determined to be defective. In Applicant claim 23, the term "locating IDDQ defects" means to localize the defect within the chip. Inoshita does not disclose a method of localizing an IDDQ defect within the chip. Inoshita discloses test methods to determine if the chip is defective or not.

Accordingly, Applicants believe that the rejected claims 9-16 are not unpatentable in view of Jennion in combination with Teene; for Claim 17, in view of Jennion in combination with Teene, and additionally in view of Cole; for Claims 19-20, in view of Jennion in combination with Teene, and additionally in view of Sagasawara; Claims 19-20, in view of Jennion in combination with Teene, and additionally in view of Sagasawara in combination with Inoshita, and respectfully request that Examiner reconsider and withdraw the stated rejection of claims 9-25 under 35 U.S.C. 103(a).

In view of the foregoing arguments and amendments, Applicant believes that she has overcome all the rejections to the application, and respectfully requests that all the amendments be entered and that the Examiner pass all the pending claims to issue.

Should the Examiner have any suggestions pertaining to the allowance of the application, the Examiner is encouraged to contact Applicant's undersigned representative at the telephone number shown below.

Respectfully submitted,
LEAH M. P. PASTEL

/ H. Daniel Schnurmann /

By: _____
H. Daniel Schnurmann, Agent
Registration No. 35,791
Tel. No. (845) 894 2481